8.3 A Non-Coherent PSK Receiver with Interference-Canceling for Transcutaneous Neural Implants

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Traditional PSK receivers usually require a phase lock loop (PLL) in carrier recovery circuits. This paper presents a non-coherent PSK receiver without a PLL by using bandpass sampling theory [1]. Digital implementation of bandpass sampling digitizes the carrier signal before sampling [2]. With the presence of jitter, however, this implementation is susceptible to error when the sampling occurs at the transition edge of the digitized carrier signal. This problem is solved by sampling the analog PSK signal with a switch-capacitor array, avoiding an abrupt amplitude change even at the zero-crossing point of the signal carrier. These samples are then processed in the analog domain, which requires no ADC for data demodulation. This scheme can tolerate 1ns of jitter equivalent to a SNR of 20dB.

With 2Mb/s data rate and 20MHz carrier frequency, this receiver is designed for transcutaneous inductively coupled data telemetry to support high data rate neural implants, e.g. 1000-electrode retinal prostheses [3]. It is required to coexist with the power telemetry in a dual-band configuration, where separate power and data carriers are used to support both high power efficiency and high data rate [4]. The power signal (1MHz), however, is a strong interference source for data transmission. This interference can be cancelled along with the analog demodulation without additional circuitry when applying Differential Phase Shift Keying (DPSK), which is chosen because DPSK requires less SNR than ASK or FSK to achieve the same BER. A "1" is coded as a 180° phase shift of the carrier frequency between the current symbol (S_n) and the one which is two symbol lengths earlier (S_{n-2}), and a "0" is coded as no phase shift.

At the receiver front-end, a passive 1st-order highpass filter and a band-limited low-gain amplifier provide bandpass filtering for the sampling circuits (Fig. 8.3.1). The sampling clock is generated by a 16MHz crystal oscillator. Eq. (1) identifies the relationship between sampling frequency (f_s), data carrier frequency (f_c), and symbol rate (f_d), ensuring that the sampling will not always occur at the zero crossing point of the carrier.

$$f_s = 4 f_c / (2n+1) = 4 k \cdot f_d \quad (n=0,1,2,\ldots; k=1,2,3,\ldots) \qquad (1)$$

Samples of S_n are compared to samples of S_{n-2}. A phase shift of 180° indicates amplitude differences between the samples of S_n and their counterparts of S_{n-2}; no phase shift indicates zero amplitude differences between these two groups. The absolute values of amplitude differences are summed by an integrator, and a bit slicer compares the total to a reference voltage and generates the binary data accordingly. The integrator is then reset for the next integration. When the frequency deviation between the external and internal crystal oscillators is 100ppm, the induced sampling error between S_n and S_{n-2} is -41dB, thus the effect of frequency deviation is negligible and no phase-tracking device, such as a PLL, is required.

In the external transmitters, a 20MHz crystal oscillator generates clocks for the data carrier frequency, 2Mb/s symbol rate, and 1MHz power carrier. Any two samples separated by two symbol periods (1μs) contain the power signal interference $A_{pwr}\cos(\omega_{1M}t+\varphi)$ and $A_{pwr}\cos(\omega_{1M}t+\varphi+2\pi)$ respectively; this interference is cancelled by taking the analog difference of these samples. This scheme can tolerate a 0.5% frequency deviation of the power interference and still keep the remaining interference below -20dB. When the data rate is a multiple m of the power carrier frequency, this method compares the current symbol to that of m symbols earlier by changing the differential coding accordingly. Furthermore, other periodic noise, such as high-order harmonics generated by transmitter amplifiers, is cancelled with the same mechanism.

In the core demodulation circuit, samples from the previous two symbols are stored on a switched-capacitor array (Fig. 8.3.2). During ph1, a new sample is stored. During ph2, $(V_{n,i} - V_{n-2,i})$ and $(V_{n-2,i} - V_{n,i})$ is performed by closing the switches in the path of the continuous line, where the subscripts n and i indicate the sequence of symbols and the sequence of samples within each symbol. The sign of $(V_{n,i} - V_{n-2,i})$ is detected using a comparator, and this sign signal controls the cross-coupled switches in front of the integrator for the integration of $|V_{n,i} - V_{n-2,i}|$. During the next ph1, $|V_{n,i} - V_{n-2,i}|$ is integrated while a new sample is stored. The differential output of the integrator is equal to the sum of the absolute difference between S_n and S_{n-2}, and is reset at every symbol edge. Before each reset, the integrator output is compared to a reference voltage using a differential latch comparator and then generates the NRZ data.

A 2MHz data clock is used to reset the integrator and is derived from a 16MHz sampling clock with 8 possible phases. The clock phase which is closest to the symbol edge is found during the preamble sequence "1,0,1,0,…". The integrator reset is first chosen arbitrarily from 8 possible phases and then shifted by one sampling period after every two symbol periods. In Fig. 8.3.3, *Vx* and *Vy* are the integrator outputs before each reset. When the integrator is reset at the middle of a symbol, $|Vx| = |Vy|$. The sign of $(|Vx| - |Vy|)$ changes whenever the reset phase passes the mid-symbol point; by detecting this sign change, the reset phase closest to the symbol edge can be located by delaying the mid-symbol phase for four sampling periods. In the worst case, the edge is captured in 17 symbol periods where all 8 possible phases are searched before finding the one closest to the symbol edge. In order to compensate for the phase drift due to crystal frequency deviation, the symbol edge is recaptured at the beginning of every data packet.

When the system starts to capture the symbol edge (Fig. 8.3.4), block "a" generates the proper digital timing signal for the operation of block "b" and the integrator reset in Fig. 8.3.2. Block "b" samples the integrator output and compares the values of *Vx* and *Vy* (Fig. 8.3.3). Once the mid-symbol point is located, the XOR output becomes high, and a pulse signal is generated to reset the DFF array in block "d". At the DFF array output, *ch4* has *4* more sample periods of delay than *ch1*. Once the symbol edge is detected, *ch4* provides the data clock for the integrator reset. Block "c" generates the control signal for the symbol edge detection circuits. Note that when the mid-symbol point is detected, the integrator output can be stored as a reference voltage of the bit slicer because it is approximately half the amplitude difference between "1" and "0".

When the signal to interference ratio is -9dB (Fig. 8.3.5), the demodulator is able to cancel the interference without a filter. The system can operate under $0.38V_{pp}$ power supply fluctuation, as fully differential circuit topology is used. The same chip can also demodulate different carrier frequencies up to 68MHz by choosing different values of n in eq. (1). Figure 8.3.6 shows a summary of the chip. The demodulator is fabricated in a 0.35μm CMOS process, with a power consumption of 6.2mW and an active die area of 2.6×1.7 mm² as illustrated in Fig. 8.3.7.

Acknowledgments:
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References:

[1] R. G. Vaughan, N. L. Scott, and D. R. White, "The Theory of Bandpass Sampling," *IEEE Trans. Signal Processing*, vol. 39, pp. 1973 – 84, Sept., 1991.

[2] M. Yuce, "A Differential-Based Multiple Bit Rate PSK Receiver: Theory, Architecture, and SOI CMOS Implementation," Ph.D. Dissertation, North Carolina State University, EE Dept., Raleigh, NC, 2004.

[3] W. Liu and M. S. Humayun, "Retinal Prosthesis," *ISSCC Dig. Tech. Papers*, pp. 218 – 219, Feb., 2004.

[4] W. Liu, et al., "Implantable Biomimetic Microelectronic Systems Design," *IEEE Engineering in Medicine and Biology Magazine*, vol. 24, pp. 66 - 74 Sept.-Oct., 2005.

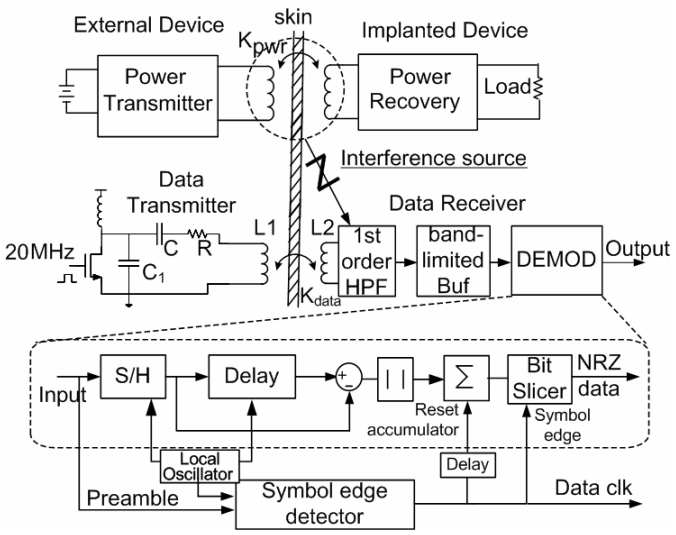

Figure 8.3.1: Overview of Telemetry System.

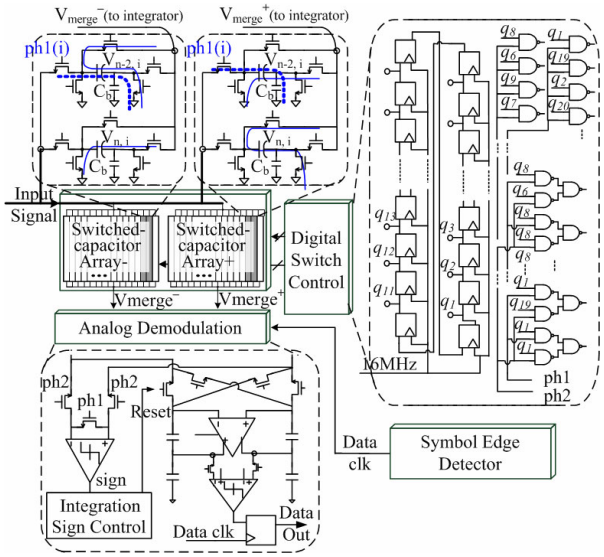

Figure 8.3.2: Circuit Implementation of the analog demodulation.

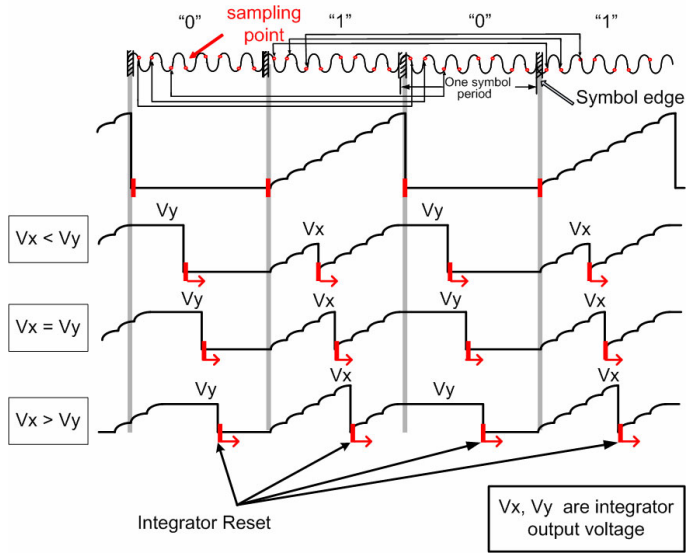

Figure 8.3.3: Output of the integrator during preamble sequence.

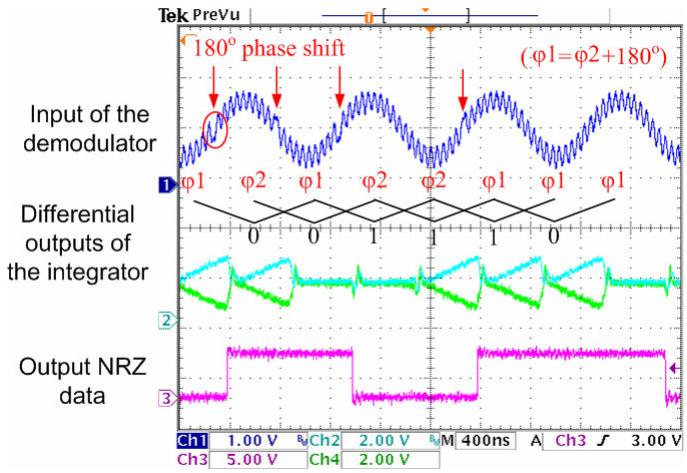

Figure 8.3.5: Test results.

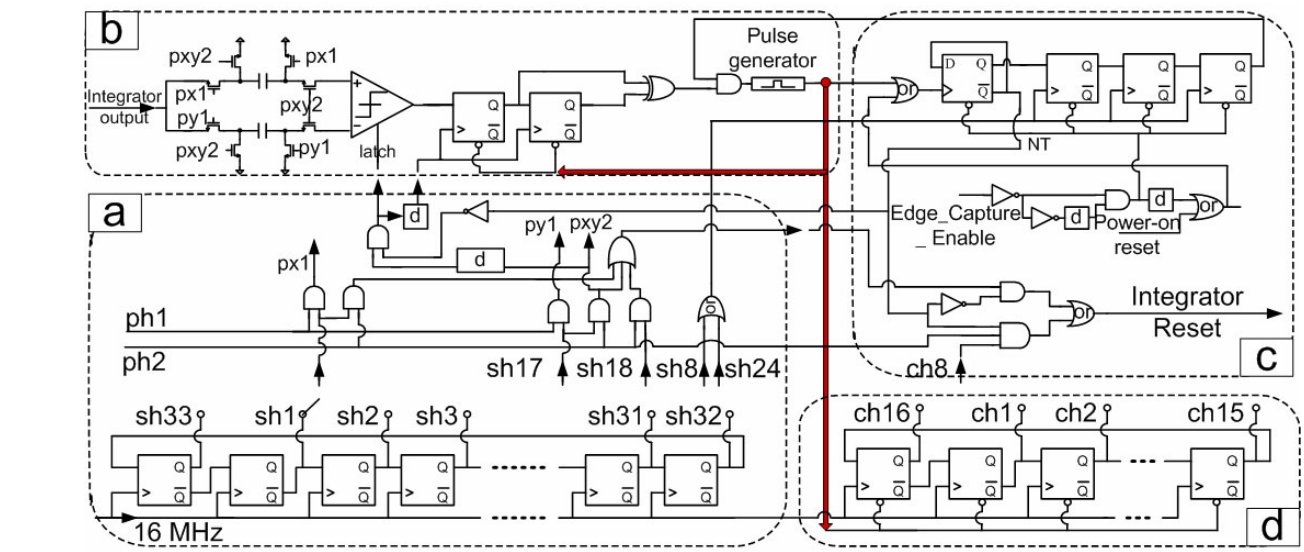

Figure 8.3.4: Circuit implementation for symbol edge detection.

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Process	0.35μm CMOS
Signal to Interference Ratio	– 9 dB
Carrier Frequency	20, 28, 36, 44, 52, 60, 68 MHz
Data Rate	1 or 2 Mb/s
Sampling Frequency	16 MHz
Active Chip Area	2.6 x 1.7 mm^2
Power Consumption	6.2 mW

Figure 8.3.6: Chip summary.

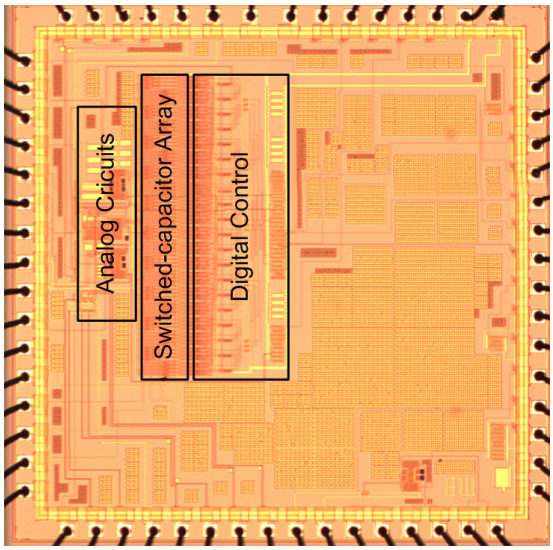

Figure 8.3.7: Chip Micrograph.

